

## CLAIMS

What is claimed is:

- 1           1.     1. A computer-implemented method comprising the steps of:
  - 2                     calculating by means of software a phase lock loop (PLL) voltage controlled
  - 3                     oscillator (VCO) output signal frequency in response to a desired output
  - 4                     clock frequency;
  - 5                     calculating by means of software a feedback divider ratio for said PLL in
  - 6                     response to said VCO output signal frequency; and
  - 7                     generating by means of software a transistor level netlist for an analog PLL
  - 8                     core, said analog PLL core having a VCO with said VCO output signal
  - 9                     frequency and a feedback divider with said feedback divider ratio;
  - 10                    laying out a semiconductor chip; said semiconductor chip
  - 11                    layout including said layout tile;
  - 12                    integrating said analog PLL core transistor level; netlist into a
  - 13                    transistor level netlist of said semiconductor chip;
  - 14                    verifying said semiconductor chip layout by comparing connections described
  - 15                    in said semiconductor chip layout against connections described in said
  - 16                    semiconductor chip transistor level netlist;
  - 17                    checking said verified layout for compliance with design rules for a
  - 18                    semiconductor chip manufacturing process; and
  - 19                    generating masks for said semiconductor chip after said verified semiconductor
  - 20                    chip layout design rule check is completed.